

Serial No.: 10/824,942
Examiner: Mohammad Timor Karimy
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Page 4 of 7

REMARKS

Reconsideration is requested in view of the above amendments and the following remarks. Editorial revisions have been made in claims 1, 2 and 5. New claim 6 has been added. The revisions and the new claim are supported by the original disclosure, for example, Figs. 1-4. No new matter has been introduced. Claims 1-6 are pending in the application.

Claim Objections

Claim 2 is objected to because of informalities. Claim 2 has been editorially revised to address the Examiner's concern.

Claim Rejections – 35 USC § 102

Claims 1 and 2 are rejected under 35 USC § 102(b) as being anticipated by Ishikura et al. (US 2002/0079556). Applicant respectfully traverses this rejection.

Claim 1 requires that a dummy layer part be disposed directly on a portion of a semiconductor substrate that is of higher resistance than a well region in circuit parts of the semiconductor substrate between a digital circuit part and an analog circuit part. For example, the higher resistance of the substrate may be caused by the increase of the distance between an n-well region in the digital circuit part and an n-well region in the analog circuit part when the dummy layer is disposed between the digital circuit part and the analog circuit part. Because of the increased resistance, the present dummy layer part helps decrease a reverse hFE of a parasitic transistor. As a result, a fluctuation of an electric potential of the n-well region in the analog circuit part as well as a parasitic current is drawn from a back gate of the analog circuit part is decreased. This helps suppress a deterioration of circuit properties of the analog circuit part (see page 3, line 34 to page 4, line 8 of the present specification).

Ishikura et al. fail to disclose a dummy layer part being disposed directly on a portion of a semiconductor substrate that is of higher resistance than a well region in circuit parts of the semiconductor substrate between a digital circuit part and an analog circuit part, as recited in claim 1. Instead, the Ishikura et al. discuss a dummy gate

Serial No.: 10/824,942
Examiner: Mohammad Timor Karimy
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Page 6 of 7

electrode being disposed directly on a dummy diffused layer which is of lower resistance (see Ishikura et al., paragraph [0077]). The focus of Ishikura et al. disclosure is to prevent the dummy diffused layer from being silicided and thus prevent the formation of a noise propagation path in the dummy diffused layer (see Ishikura et al., paragraph [0081]), rather than increasing the resistance of the p-type substrate between the digital and the analog sections. In fact, Ishikura et al. is complete silent as to the dummy gate electrode increasing the resistance of the p-type substrate between the digital and the analog sections.

Claim 2 requires a dummy diffused region between a dummy layer part and one of an analog circuit part and a digital circuit part. With the present dummy diffused region, most of a collector current of a parasitic transistor formed in the semiconductor integrated circuit can be supplied from the dummy diffused region. As a result, the fluctuation of an electric potential of an n-well region in the analog circuit part is further decreased and thus a deterioration of circuit properties of the analog circuit part is further suppressed.

Ishikura et al. fail to disclose a dummy diffused region between a dummy layer part and one of an analog circuit part and a digital circuit part as recited by claim 2. The Ishikura et al. dummy diffused layers are in fact covered by dummy gate electrodes and disposed between STIs (shallow trench isolations), as shown in Figs. 3B, 4B, 5B, rather than between the dummy layer part and one of the analog circuit part and digital circuit part as required by claim 2. In addition, since the Ishikura et al. dummy diffused layers are disposed under the dummy gate electrodes, the layout of the dummy diffused layers is limited by the layout of the dummy gate electrodes. Therefore, unlike the present semiconductor integrated circuit, the capability for reducing the size of the Ishikura et al. semiconductor device is substantially limited. For at least these reasons, claim 2 is patentable over Ishikura et al.

Serial No.: 10/824,942
Examiner: Mohammad Timor Karimy
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Page 6 of 7

Claim Rejections – 35 USC § 103

Claims 3 and 5 are rejected under 35 USC 103(a) as being unpatentable over the prior art admitted by Hasegawa (US 5,900,927) in view of Ishikura et al. Applicant respectfully traverses this rejection.

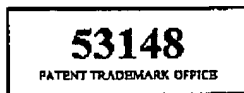
Claim 3 depends from claim 1 and is patentable over the prior art admitted by Hasegawa in view of Ishikura et al. for at least the same reasons discussed above regarding claim 1. The prior art admitted by Hasegawa does not remedy the deficiencies of Ishikura et al. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claim.

Claim 5 requires a dummy layer part to be disposed directly on a semiconductor substrate that is of higher resistance than one of a well region in the circuit parts of the semiconductor substrate between a digital circuit part and an analog circuit part. Claim 5 is patentable over the prior art admitted by Hasegawa in view of Ishikura et al. for reasons similar to those discussed above regarding claim 1. The prior art admitted by Hasegawa does not remedy the deficiencies of Ishikura et al. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claim.

Claim 4 is rejected under 35 USC 103(a) as being unpatentable over Hasegawa's admitted prior art in view of Hasegawa. Applicant respectfully traverses this rejection. In view of the dependence of claim 4 on claim 3, Applicant assumes that the rejection intended to include Ishikura et al. as one of the references. Claim 4 depends from claim 3 and is patentable over the prior art admitted by Hasegawa in view of Ishikura et al., and further in view of Hasegawa for at least the same reasons discussed above regarding claim 3. Hasegawa does not remedy the deficiencies of Ishikura et al. Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claim.

Serial No.: 10/824,942
Examiner: Mohammad Timor Karimy
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Page 7 of 7

In view of the above, favorable reconsideration in the form of a notice of allowance is respectfully requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612) 455-3804.



Dated: January 10, 2007

DPM/cy

Respectfully submitted,

HAMRE, SCHUMANN, MUELLER &
LARSON, P.C.
P.O. Box 2902-0902
Minneapolis, MN 55402-0902
(612) 455-3800

By: 

Douglas P. Mueller
Reg. No. 30,300